

Model-Order Reduction of High-Speed Interconnects: Challenges and Opportunities

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The ongoing drive in the very large-scale integration industry for higher operating frequencies has made interconnects a dominant factor in the overall system performance. Interconnect effects, such as crosstalk, ringing, delay, and ground bounce could have a detrimental effect on signal integrity. If not accurately characterized and compensated for at earlier design iterations, these impairments can severely degrade the performance of high-speed designs. At high frequencies, interconnects behave as coupled distributed multiconductor transmission lines (MTLs) described by partial differential equations. Signal integrity analysis typically requires using SPICE-like circuit simulators to determine signal propagation. One of the main challenges which arises therein is related to the problem of incorporating MTL macromodels into circuit simulators; which are essentially ordinary differential equations solvers. In addition, these macromodels have to satisfy additional constraints such as stability, causality and passivity. Several methods have been proposed in the literature for macromodeling of high-speed interconnects. In general, these macromodels can be described in the form of a large number of lumped components and appropriate delay sources that capture the behavior of the MTLs over a large frequency range. This often leads to a large equivalent circuit, whose simulation is computationally expensive and sometimes not feasible particularly in the case of a large number of coupled lines. Although model-order reduction has been proposed to reduce the complexity of the resulting macromodels, several impediments are still to be resolved.

In this talk, recent advances and outstanding challenges in model reduction and simulation of high-speed interconnect circuits will be presented.