Model Order Reduction in VLSI ASIC Design: What We Use, What We Want, and Why

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One of the industrial "success stories" for model-order-reduction algorithms is found in analysis tools for design of application-specific VLSI integrated circuits. This talk will begin by discussing the application domain, the types of starting systems it generates, how reduced-order-models interact with the rest of the analysis system, and system requirements for algorithmic performance.

Moment-matching algorithms of one form or other are a common choice for base algorithm in current electronic design automation tools. We will discuss why they are a good match for VLSI interconnect and why alternative techniques have had difficulties making inroads in this application. We have recently shown that some more "heuristic" methods developed in the design-automation community can be precisely related to the more general Krylov-projection methods. This connection suggests an alternative class of algorithms that can have significant performance advantages in systems like VLSI interconnect that have underlying sparse topologies, so we will speculate on some novel applications and present some open challenges uncovered in industrial deployment of such approaches.

Finally, we will discuss a problem that may be suitable for application of currently-available technology for reduction of nonlinear systems, discuss verification and validation of the models produced, and show some initial results.